

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

HAYSTACK OBSERVATORY

WESTFORD, MASSACHUSETTS 01886

Phone: (978) 692-4764
Fax: (781) 981-0590

27 July 2000

To: A. Rogers
From: W. Aldrich
Subject: SRT Digital Receiver

In attempting to flesh out the block diagram of the SRT digital receiver, I have stumbled across a few vexing details.

Briefly, these are:

The Basic Stamp is limited to a total of 16 programmable pins, eight of which are already used on the existing analog receiver.

Booting through the IDMA port requires a 16 bit wide data/address connection. Booting through the serial port requires a separate monitor program to be running. Booting through the Byte DMA port requires the Basic Stamp to emulate a byte wide prom.

The parameter space of the 4014 (Digital receiver) is accessed through a parallel port with five address bits and eight data bits. This is most naturally done by connecting to the I/O port of the 2189M, but that connection precludes use of the IDMA port on the 2189M because of dual mode pin conflicts on the 2189M.

The 2189M cannot be directly driven by pins from the Basic Stamp because the stamp Voh exceeds the allowable Vih of the 2189M.

All of these problems can be addressed, but I have not been able to find a solution which adds no components to the design. If you are willing to add components, I present two possibilities which are shown in figures 1 and 2. I'm sure there are other possibilities, but these two seem to be in the spirit of low cost and low power which the SRT receiver requires.

Figure 1 shows the addition of a "bus switch" which allows the stamp to drive the 2189M. There is no logical function in the bus switch, it merely limits the maximum input voltage to the 2189M and is bi-directional so full swing signals from the 2189M will be properly interpreted by the stamp. A boot prom is also added which holds only the code which sets up the byte dma and the monitor which allows the processing program to be input through the serial port from the stamp. Although this leads to some software complexity, it does allow most of the code to be input from the stamp and allows the 2189M to be configured in the full memory mode. The 4014 parameter space appears naturally within the I/O space of the 2189M.

Figure 2 is an alternate approach which attempts to solve all of the problems with a programmable Xilinx device. This cpld is 5 volt compliant so it can withstand the high voltages of the stamp while dealing with the lower voltages required by the other chips. The cpld contains logic which allows a bi-directional serial to parallel conversion in order to couple the serial data streams from the stamp to the IDMA port of the 2189M. All software is loaded through the stamp and no monitor program is required. In fact, all program memory and data memory is available to the stamp by way of the IDMA port. The cpld also contains an address latch to allow the parameter space of the 4014 to be accessed from the I/O port of the 2189M.

The component costs for the two approaches are similar, and the pin counts are also similar. The boot prom and the latch are probably around \$5.00 each. (The boot prom would have to be socketed.) The Xilinx part is \$3.75 for the quad flatpack package. It comes as an in-circuit programmable part so it can be soldered on the board.

I believe that the software differences might determine which approach is best. How can we make that determination?