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To: Mark 5 Development Group
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Subject: MARK 5B I/O BOARD Physical Description

INTRODUCTION

The Mark 5B I/O board is a VSI compatible PCI board, which has VSI input and output connections as well as the ability to transfer data on the FPDP bus between itself and a StreamStor disk controller. The board is controlled by software that communicates via the PCI bus to set the parameters of operation and the details of data handling.

The Mark 5B I/O board is a full length PCI board that plugs into a PCI 32 bit/33MHz socket on a PC motherboard.

The Mark 5B I/O board also drives a panel of eight LED indicators, which are mounted on the front of the Mark 5 chassis. These indicators reflect the operating mode of the board and allow visual monitoring of the board activity.

PHYSICAL DESCRIPTION

Figure 1 shows a component side view of the board and serves to show the locations of features described in the following text.

J27 is an MDR-80 connector that is positioned to appear at the back bulkhead of the host PC. This is the VSI input connector. All signals on this connector are differential LVDS inputs. A second MDR-80 connector appears at the top right of the board (J28). This is the VSI output connector. All pins on this connector are differential LVDS outputs. The detailed signal identities are given in the section entitled "connections" and are in accordance with the VSI-H specification. In some applications of the Mark 5B I/O board there are inputs associated with the VSI data outputs. These signals appear on the MDR-14 connector (J15) immediately to the right of the VSI output connector.

J1, at the top of the board, is the FPDP connector. The signals on this connector are bi-directional and are primarily at TTL levels, the exception being the differential PECL clock signals. The FPDP bus operates in a half duplex manner and its direction is controlled by the StreamStor board.

J13 and J14 (at the top left side of the board) and J12 on the right edge are diagnostic connections that are not used in normal operation.

The edge connector (J16) is the 32/33 PCI connector which is plugged into the motherboard socket.

The small pin field labeled J18 (between the FPDP connector and the MDR-80 at the top of the board) serves to connect the indicator LED panel to the board.

J29 and J30 (SMB coax connectors near the FPDP connector) are outputs "DOT Monitor" and "ROT Monitor" respectively. The coax connector J31 (near the VSI input connector) is an input connector for an alternate "1 PPS" signal.

The large 168-pin connector labeled J17 holds the SDRAM, which is required for DOM configurations.

U23 (close to the PCI connector) is a PLX 9030 that realizes the PCI interface between the motherboard and the Mark 5B I/O board. The Mark 5B I/O board is a PCI “target” which never takes control of the PCI bus. It does, however, actively assert a PCI interrupt. The operational parameters for the PLX chip are stored in an EEPROM located at U9.

U7 (partially behind the SDRAM module) is a Xilinx FPGA that holds the functionality of the board. It is configured on power up by the EEPROMs U24, U25, and U26. These EEPROMs are in turn loaded by the software from the motherboard and can hold either DIM or DOM configurations, but only one at a time.

VSI INPUT PINS

The signals on the VSI input connector (J27) conform to the requirements of the VSI-H specification and are also specified in Table 1 below.

Signal	Pin (+)	Pin (-)	Comments
BS0	1	2	
BS1	3	4	
“	“	“	
“	“	“	
BS14	29	30	
BS15	31	32	
BS16	42	41	
BS17	44	43	
“	“	“	
“	“	“	
BS30	70	69	
BS31	72	71	
1PPS	33	34	
Unused	35	36	
PVALID	37	38	
CLOCK	39	40	
PCTRL	74	73	
PDATA	76	75	
PSPARE1	78	77	Spare signal 1
PSPARE2	80	79	Spare signal 2

Table 1: VSI Input Pin Allocations

VSI OUTPUT PINS

The signals on the VSI output connector (J28) conform to the requirements of the VSI-H specification and are also specified in Table 2 below

Signal	Pin (+)	Pin (-)	Comments
RBS0	1	2	
RBS1	3	4	
“	“	“	
“	“	“	
RBS14	29	30	
RBS15	31	32	
RBS16	42	41	
RBS17	44	43	
“	“	“	
“	“	“	
RBS30	70	69	
RBS31	72	71	
R1PPS	33	34	
ROT1PPS	35	36	
QVALID	37	38	
RCLOCK	39	40	
QCTRL	74	73	
QDATA	76	75	
QSPARE1	78	77	Spare signal 1
QSPARE2	80	79	Spare signal 2

Table 2: VSI output pin allocations

FPDP PINS

The signals on the FPDP connector (J1) conform to the requirements of the FPDP specification and are also listed in the table below. Cable conductor numbers are shown in brackets. These numbers also correspond to the FPDP symbol on the Mark 5B I/O board schematics. These signals are primarily single ended TTL and are indicated with a "*" suffix when they are active low. (PSTROBE and PSTROBE* are differential PECL.)

Pin	Row A	Row B	Row C	Row D
1	GND (1)	NC (2)	GND (3)	GND (4)
2	GND (5)	GND (6)	NRDY* (7)	GND (8)
3	DIR* (9)	GND (10)	NC (11)	GND (12)
4	SUSPEND (13)	GND (14)	II (15)	GND (16)
5	PIO2 (17)	GND (18)	GND (18)	GND (20)
6	NC (21)	GND (22)	NC (23)	GND (24)
7	PSTROBE (25)	GND (26)	PSTROBE* (27)	GND (28)
8	SYNC* (29)	GND (30)	DVALID* (31)	GND (32)
9	D31 (33)	D30 (34)	GND (35)	D29 (36)
10	D28 (37)	GND (38)	D27 (39)	D26 (40)
11	GND (41)	D25 (42)	D24 (43)	GND (44)
12	D23 (45)	D22 (46)	GND (47)	D21 (48)
13	D20 (49)	GND (50)	D19 (51)	D18 (52)
14	GND (53)	D17 (54)	D16 (55)	GND (56)
15	D15 (57)	D14 (58)	GND (59)	D13 (60)
16	D12 (61)	GND (62)	D11 (63)	D10 (64)
17	GND (65)	D09 (66)	D08 (67)	GND (68)
18	D07 (69)	D06 (70)	GND (71)	D05 (72)
19	D04 (73)	GND (74)	D03 (75)	D02 (76)
20	GND (77)	D01 (78)	D00 (79)	GND (80)

Table 3: FPDP pin allocations.

POWER

Power for the Mark 5B I/O board is drawn entirely through the PCI connector. The bulk of the power is obtained at +5 Volts. The +12 Volt supply is used to power the LED indicators. Total board power is estimated at 23 Watts. The +5 Volt supply delivers about 22 Watts, the +12 Volt supply delivers 1 Watt.

The current from the +5 Volt supply passes through jumpers J10 and J11. These jumpers should both be in place during normal board operation.

The current from the +12 Volt supply passes through jumper J4. This jumper must be in place for the LED indicators to operate.

FUNCTIONALITY

The functionality of the Mark 5B I/O board is primarily realized by the operation of the FPGA. The FPGA is a Xilinx Virtex II Pro (type 2VP30). The FPGA is in a 896-ball grid array package located at position U7.

CONFIGURATION

This device is a RAM based FPGA and as such will not retain its functionality when the power is off. Consequently, it re-loads its configuration from the non-volatile EEPROMS whenever the power is applied. It is also possible for software to command a reloading of the configuration provided pins 2 and 3

of J26 are jumpered together. If pins 1 and 2 of J26 are jumpered together instead, then configuration will take place in response to the push button S1.

The software operating on the motherboard normally downloads the configuration that is resident in the non-volatile EEPROMS. This configuration need be loaded only once, as it will be retained in the EEPROMS for use each time power is cycled. A new configuration may be loaded into the EEPROMS to change the functionality of the FPGA (from a DOM to a DIM for example).

DOM OPERATION

When in DOM configuration, the Mark 5B I/O board is able to read disk data from the FPDP bus, manipulate it according to control parameters, and output the manipulated data to the VSI output connector. In addition it is able to extract phase cal information from the incoming data streams.

DIM OPERATION

The DIM configuration is used to take data streams from the input VSI connector, select a subset (or possibly all) of the data streams, append headers with timing information, and write the resultant data efficiently to the disks via the FPDP bus. In addition it is able to extract phase cal information from the incoming bit streams.

CONTROL & SETUP

Operating control and setup of the Mark 5B I/O board is accomplished through the software running on the motherboard. The board appears in the address space of the PCI bus. The details of the parameters and procedures are specified in Mark 5 memos 24.3 (DIM) and 26 (DOM) which are found on the Haystack website at

[ftp:// web.haystack.edu/pub/mark5/index.html](ftp://web.haystack.edu/pub/mark5/index.html).

JUMPER SETTINGS and TEST POINTS

Table 4 specifies the jumper settings for normal operation. J2 through J11 are two pin headers which are either joined by a shorting plug (Present) or left open (Open). J22 through J26 are three pin headers, which may have a shorting jumper between pins 1 and 2 (1 to 2) or between pins 2 and 3 (2 to 3).

J	Schematic Sheet	Normal Pos.	Description
2	2	Present	Board power dissipation is
3	2	Open	specified by J2 and J3 to be 25-Watts Max.
4	2	Present	12 Volt connection for LED's on indicator panel
5	3	Open	DXP (Pin 1) DXN (Pin 2) (Temp. diode for FPGA)
6	3	Present	Forces M0 = "0"
7	3	Present	Forces M1 = "0"
8	3	Present	Forces M2 = "0" (M0 + M1 + M2 = 0) => Slave serial
9	8	Open	Pin1 is test point for Clock Gen.
10	9	Present	+5 Volt Jumper
11	9	Present	+5 Volt Jumper
22	3	2 to 3	TDI received from PCI bus via PLX chip
23	3	2 to 3	TMS received from PCI bus via PLX chip
24	3	2 to 3	TCK received from PCI bus via PLX chip
25	3	2 to 3	TDO received from PCI bus via PLX chip
26	3	2 to 3	PROG_B received from PCI bus via PLX chip

Table 4: Jumper settings for normal operation

Table 5 gives the nominal voltage to be found on the “red loop” test points. The “black loop” test points are at the ground reference potential

JP	Voltage
1	+5 Volts
2	+3.3 Volts
3	+2.5 Volts
4	+1.5 Volts
5	GND
6	GND
7	GND
8	GND

Table 5: DC power test points.

There are five board mounted LED’s which sense various voltages and conditions. These are given in table 6.

D	Schematic Sheet	Description
1	3	“Done”, Light implies FPGA is configured
2	9	+2.5 Volt supply is on
3	9	+1.5 Volt supply is on
4	9	+5 Volt supply is on (back of board)
5	9	+3.3 Volt supply is on (back of board)

Table 6: On board indicator LED’s

